IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A processor, comprising:

a cache capable of storing data;

a control logic capable of controlling a flow of data; and

at least one core coupled to the cache and the control logic, ~~capable of generating a multiple of a CPU clock signal having,~~ the at least one core comprising:

an instruction cache capable of storing data;

an instruction fetch unit capable of fetching data;

a plurality of integer execution units coupled to the instruction fetch unit, each integer execution unit generating, in response to the data, an output signal at a first frequency, the first frequency being a frequency of the CPU clock signal;

a plurality of latches, each latch connected to receive the output signals from the integer execution units;

a merge unit, the merge unit generating a merged signal containing the output signals at a second frequency, the second frequency being a multiple of the first frequency; and

a ~~single~~ floating point graphics unit, the floating point graphics unit comprising logic for processing the merged signal at the second frequency, the processing comprising performing floating point arithmetic operations ~~coupled to the plurality of integer execution units including circuitry capable of generating the multiple of the CPU clock signal~~.

2. (Currently amended) ~~A processor~~ The processor of claim 1, wherein the merge unit comprises ~~further comprising~~ a delay-locked loop (DLL) circuit having a charge pump, the DLL circuit being capable of generating ~~the multiple of the CPU clock signal~~ a clock signal at the second frequency.

3. (Currently amended) ~~A processor~~ The processor of claim 2, wherein the DLL circuit comprises a voltage control delay line unit capable of generating multiple delayed clock signals.

4. (Currently amended) ~~A processor~~ The processor of claim 2, wherein the DLL circuit further comprises a control signal capable of ~~controlling~~ delaying the CPU clock signal by propagating the CPU clock signal through a plurality of inverters.

5. (Canceled)

6. (Currently amended) ~~A processor~~ The processor of ~~claim 2~~ claim 3, wherein the DLL circuit further comprises at least one symmetric NOR and one symmetric NAND capable of combining signals.

7. (Currently amended) ~~A processor~~ The processor of ~~claim 3~~ claim 6, wherein the voltage control delay line unit ~~further~~ comprises a delay unit having at least two inverters capable of delaying the CPU clock signal.

8. (Currently amended) ~~A processor~~ The processor of claim 7, wherein a first delayed clock signal and a last delayed clock signal ~~signals~~ from ~~at least two inverters~~ the voltage control delay line unit are ~~manipulated into a control signal~~ compared by a phase frequency detector and converted into a control signal by the charge pump.

9. (Canceled)

10. (Currently amended) ~~A processor~~ The processor of ~~claim 2~~ claim 8, wherein the DLL circuit further comprises a ~~charge pump having a~~ Schmitt circuit, capable of increasing or decreasing a voltage of the control signal.

11. (Canceled)

12. (Currently amended) ~~A processor~~ The processor of claim 1, wherein the multiple of the CPU clock signal comprises a higher frequency clock having a higher frequency than the CPU clock signal.

13. (Currently amended) ~~A processor~~ The processor of claim 1, wherein the single floating-point graphics unit comprises a multiplier pipeline and an adder pipeline.

14. (Currently amended) A ~~circuit, comprising: a~~ floating point graphics unit for processing multiple integer execution unit input signals in a single cycle of a CPU clock signal, the floating point graphics unit ~~having,~~ comprising:

a voltage control delay line unit capable of generating multiple delayed clock signals from the CPU clock signal, the multiple delayed clock signal including a first signal and a last signal;

a plurality of pulse generators each generating a pulse signal timed in accordance with one of the delayed clock signals;

a phase frequency detector coupled to the voltage control delay line unit capable of detecting phase differences between the first signal and the last signal, the phase frequency detector generating a phase frequency detector output;

a charge pump coupled to the phase frequency detector and the voltage control delay line unit capable of increasing or decreasing ~~voltage~~ a control signal voltage in response to the phase frequency detector output;

~~at least one~~ at least one symmetric NOR gate and at least one symmetric NAND gate coupled to the voltage control delay line unit capable of combining a plurality of the pulse signals ~~with identical rising edges; at least one symmetric NAND coupled to the at least one symmetric NOR capable of combining signals~~ and generating an output clock signal having a frequency that is a multiple of the CPU clock signal ~~with identical falling edges~~; and

a buffer ~~coupled to the at least one symmetric NAND~~ capable of buffering ~~a multiple of a CPU~~ the output clock signal and generating a buffered ou0tput clock signal, the buffered output clock signal driving the floating point graphics unit.

15. (Canceled)

16. (Currently amended) ~~A circuit~~ The floating point graphics unit of claim 15, ~~further comprising~~ wherein the voltage control delay line unit comprises a plurality of inverters capable of delaying the CPU clock signal.

17. (Currently amended) ~~A circuit~~ The floating point graphics unit of claim 14, wherein [[a]] the control signal voltage ~~capable of controlling the CPU clock signal~~ is an analog value.

18. (Currently amended) ~~A circuit~~ The floating point graphics unit of ~~claim 15~~ claim 14, wherein the output clock signal has a frequency that is a ~~the~~ multiple of a frequency of ~~the CPU clock signal is a higher frequency than~~ the CPU clock signal.

19. (Currently amended) A method for generating a custom clock frequency comprising:

receiving a CPU clock signal;

delaying the CPU clock signal with at least two inverters to generate a plurality of delayed CPU clock signals;

generating a plurality of output signals from the delayed CPU clock signals; and

combining ~~a plurality of signals from~~ the plurality of output signals to generate a combined custom clock signal, the combined custom clock signal having a frequency that is a multiple of a frequency of the CPU clock signal.

20. (Currently amended) ~~A method~~ The method of claim 19, further comprising regulating a control signal with a first signal and a last signal from the plurality of delayed CPU clock ~~output~~ signals.